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Proteus VSM for PIC18

System Level Simulation for Microchip Technologies™ PIC18 Variants.

Summary

Proteus Virtual System Modelling (VSM) combines mixed mode SPICE circuit simulation, animated components and microprocessor models to facilitate co-simulation of complete microcontroller based designs.The 'Proteus VSM for PIC18' product includes the following main software modules:

- Professional Schematic Capture module
- ProSPICE professional Simulation Engine
- All supported VSM microcotroller variants in the PIC18 Family.
- All of the Proteus Embedded Simulation Peripheral Libraries.
- VSM Studio IDE with automatic compiler configuration.
- Over 10,000 standard simulation models.

⚠ *Proteus VSM for PIC® Bundle products are ideal if you need to simulate more than one family of PIC micro-controllers.*

Variants

The following is a current list of supported variants in the PIC18 family:

- PIC18F242, PIC18F252, PIC18F442, PIC18F452
- PIC18F248, PIC18F258, PIC18F448, PIC18F458
- PIC18F1220, PIC18F1320, PIC18F2220, PIC18F2331
- PIC18F2320, PIC18F2410, PIC18F2420, PIC18F2431
- PIC18F2510, PIC18F2515, PIC18F2520, PIC18F2525
- PIC18F2610, PIC18F2620, PIC18F4220, PIC18F4320
- PIC18F4331, PIC18F44J10, PIC18F45J10, PIC18F24J10
- PIC18F25J10, PIC18F4410, PIC18F4420, PIC18F4431
- PIC18F4510, PIC18F4515, PIC18F4520, PIC18F4525
- PIC18F4610, PIC18F4620, PIC18F6520, PIC18F6585
- PIC18F8585, PIC18F8680, PIC18F6620, PIC18F6680
- PIC18F6720, PIC18F8520, PIC18F8620, PIC18F8720
- PIC18F8722, PIC18F8627, PIC18F8622, PIC18F8527
- PIC18F6722, PIC18F6627, PIC18F6622, PIC18F6527
- PIC18F6628, PIC18F6723, PIC18F23K20, PIC18F24K20
- PIC18F25K20, PIC18F26K20, PIC18F43K20, PIC18F44K20
- PIC18F45K20, PIC18F46K20, PIC18F2450, PIC18F2455
- PIC18F2458, PIC18F2550, PIC18F2553, PIC18F4450
- PIC18F4455, PIC18F4458, PIC18F4550, PIC18F4553
- PIC18F13K50, PIC18F14K50, PIC18LF13K50, PIC18LF14K50
- PIC18F2480, PIC18F2580, PIC18F4480, PIC18F4580
- PIC18F2585, PIC18F2680, PIC18F4585, PIC18F4680
- PIC18F2682, PIC18F2685, PIC18F4682, PIC18F4685
- PIC18F46J13, PIC18F47J13, PIC18LF46J13, PIC18LF47J13
- PIC18F25K80, PIC18F26K80, PIC18F45K80, PIC18F46K80
- PIC18F65K80, PIC18F66K80, PIC18LF25K80, PIC18LF26K80
- PIC18F1230, PIC18F1330, PIC18F2423, PIC18F2523
- PIC18F4423, PIC18F4523, PIC18F6390, PIC18F6490
- PIC18F8390, PIC18F8490, PIC18F6393, PIC18F6493
- PIC18F8393, PIC18F8493, PIC18F63J90, PIC18F64J90
- PIC18F65J90, PIC18F83J90, PIC18F84J90, PIC18F85J90
- PIC18F13K22, PIC18F14K22, PIC18LF13K22, PIC18LF14K22
- PIC18F2221, PIC18F2321, PIC18F4221, PIC18F4321
- PIC18F23K22, PIC18F24K22, PIC18F25K22, PIC18F26K22
- PIC18LF23K22, PIC18LF24K22, PIC18LF25K22, PIC18LF26K22
- PIC18F43K22, PIC18F44K22, PIC18F45K22, PIC18F46K22
- PIC18LF43K22, PIC18LF44K22, PIC18LF45K22, PIC18LF46K22
- PIC18F65K22, PIC18F66K22, PIC18F24K50, PIC18F25K50
- PIC18F45K50, PIC18LF24K50, PIC18LF25K50, PIC18LF45K50
- PIC18F67K22, PIC18F85K22, PIC18F86K22, PIC18F87K22
- PIC18F24J50, PIC18F25J50, PIC18F26J50, PIC18LF24J50
- PIC18LF25J50, PIC18LF26J50, PIC18F44J50, PIC18F45J50
- PIC18F46J50, PIC18LF44J50, PIC18LF45J50, PIC18LF46J50
- PIC18F26J53, PIC18F27J53, PIC18LF26J53, PIC18LF27J53
- PIC18F46J53, PIC18F47J53, PIC18LF46J53, PIC18LF47J53
- PIC18F26J13, PIC18F27J13, PIC18LF26J13, PIC18LF27J13
- PIC18LF45K80, PIC18LF46K80, PIC18LF65K80, PIC18LF66K80

Features

We believe our simulation models are the most accurate and the most complete on the market today. A summary of model capabilities is listed below:

- Fully simulates the entire instruction set.
- Supports all port and other I/O pin operations.
- Supports all timers including watchdog timer, sleep mode and wake-up from sleep.
- Supports Deep Sleep mode including independent watchdog timer and wake up from WDT, RTCC, ULPWM, INT0 and MCRL.
- Supports all Capture-Compare-PWM (CCP) modules in all modes and ECCP modules.
- Supports Parallel Slave Port (PSP) module on appropriate devices.
- Supports Parallel Master Port (PMP) module on appropriate devices.
- Supports MSSP in both the SPI mode and the I2C master and slave modes.
- Supports Analogue-to-Digital Conversion (ADC) module inc. support for voltage reference pins.
- Supports Analogue Comparator modules inc. support for internal and external voltage references.
- Supports CTMU, Charge Time Measurement Unit. All modes are simulated.
- Supports ULPWU, Ultra low-power wake-up input.
- Supports REFO, Reference Clock Output.
- Supports RTCC, Real-Time Clock and Calendar.
- Supports SRLatch module.
- Supports DSM, Data Signal Modulator on appropriate devices.
- Supports USART in all modes and EUSART for appropriate variants.
- Supports Universal Serial Bus (USB) on appropriate devices.
- Supports internal code and data EEPROM memory inc. code protection and data persistence.
- Supports Peripheral Pin Select (PPS) on appropriate devices.
- Supports Open-Drain Outputs capability on appropriate devices.
- Supports all interrupt modes.
- Event timing accurate to one clock period.
- Provides internal consistency checks on code (e.g. execution of invalid op-codes, illegal memory accesses, stack overflow checking, etc.).
- Fully integrated in to the VSM source level debugging system.
- Fully integrated into the Proteus Diagnostic Control System.

Limitations

The following is a listing of known limitations in the current version of the PIC18:

- The External Memory Interface (EMI) of devices such as the PIC18F8X20 is not modelled. These devices can only be modelled when the PMx configuration bits select the Microcontroller Mode (MC) mode of operation. Specifically, the Microprocessor Mode (MP), Microprocessor with Boot Block Mode (MPBB) and Extended Microcontroller Mode (EMC) modes are not supported.
- Power Managed Modes is not modelled. Specifically, the use of IDLEN and SCS/SCSx bits in the OSCCON register to switch oscillator sources and the behaviour of the SLEEP command is not modelled. The SLEEP command always puts the processor in to full sleep mode. This limitation is largely due to poor documentation on how the power managed modes actually affect peripherals.
- Brown-out detection and High-Low Voltage Detect (HLVD) is not modelled.
- RELEASE bit effects and Brown-out wakeup from Deep Sleep mode are not modelled.
- The Internal/External Switch Over (IESO configuration bit) and the Fail Safe Clock Monitor (FSCM configuration bit) are not modelled.
- The CAN/ECAN module is not currently modelled.
- The SPP (Streaming Parallel Part) of the USB variants is not currently modelled.
- Isochronous USB transactions in the USB variants is not currently modelled.
- The external programming interface (PGC/PGD pins) are not modelled.
- The DMA features for SPI2 PGD pins are not modelled.
- The PMDx registers effects are not modelled.
- The VREGCON register effects are not modelled.
- The ACTCON register effects are not modelled.
- The SRLCON register effects are not modelled.

Compilers

Supported Third Party Compilers

Proteus VSM models will fundamentally work with the exact same HEX file as you would program the physical device with. However, far more debugging information is available when using a compiler to write the firmware and providing these object files to Proteus in place of the HEX file provides a much richer working environment.

We recommend you use the free Labcenter VSM Studio IDE. This will greatly simplify the task as it will automatically configure supported compilers to work with a Proteus VSM simulation.

If you prefer to work inside your own IDE then you will need to set your compiler options manually. After compiling for debug, all you need to do is specify the debug file from the compiler as the program property of the microcontroller on the schematic.

VSM Studio supported toolchains

- IAR
- HI-TEC
- Microchip XC8
- Microchip XC16
- Proton+
- CCS
- Source Boost
- Byte Craft

With continual development on the Proteus Design Suite we endeavour to keep all content updated with the latest product details. On rare occasions this may not happen immediately, and website content will then be incomplete or inaccurate. We will attempt to correct any such errors as soon as possible, E&OE.