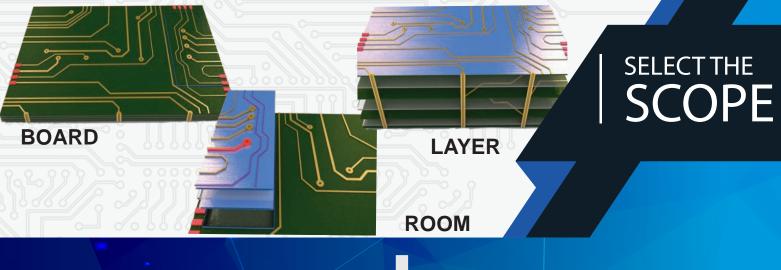


DESIGN RULE MANAGER.

The Proteus Design Suite includes a comprehensive design rule system which allows users to quickly and easily define board constraints for their designs. Design rules can be applied to different areas of the PCB and electrical filters can be applied for additional flexibility. This provides a simple but scalable way to control clearances on the PCB.



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APPLY THE FILTERS

To all objects in the scope

Between objects in one net class and other net classes

To traces and pads in a particular net class







Graphic

15th

15th

15th

15th

15th

Edge

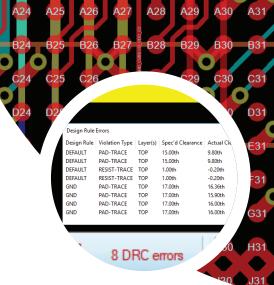
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Design rules are a vital step in defining the requirements for a PCB. They specify the allowable clearances between objects on the layout and allow the PCB editor to check or enforce these clearances when you are working on the design.

The design rule manager in Proteus is simple, scalable and flexible. Users start with a simple default rule that applies to the entire board and they can then add additional rules via the design rule manager dialogue form.

ncreasing Priority Class Class Rule Class Class Layer Rule Room Rule Class Room Class Class Room Rule New rules can be applied to

Board Rule (Default)

Laver Rule

Class Rule

Class Layer Rule

a smaller area of the board and/or they can be applied to a subset of signals such as only to a specific net class.

For example, on a multilayer PCB you often need less space between objects on inner layers than on the two outer layers. This can be handled by applying rules limited in scope to layers of the board.

Similarly, the pain of routing fanout traces to escape from a BGA is much reduced by the ability to specify a room around the fanout area and then defining a design rule with smaller clearances inside it. In this case, the scope of the rule is reduced to a small area on the PCB.

Design Rules | Net Classes | Defaults |

Region Board

⊟ Inner 2

i Inner 5 ⊞- Inner 6

⊞ Inner 7

⊞ Inner 8

⊞ Inner 9

⊞ Inner 10

BGA Escape

Rules

Rule Name

HIGHPOWER

VLCVIDEO

TOP ROUTES 5th

Clearances

8th

6th

Pad - Pad Clearance:

Pad - Trace Clearance:

Graphics Clearance:

Trace - Trace Clearance: 6th

POWER

CVBS

Pad-Pad Pad-Trace Trc-Trc

6th

6th

6th

6th

6th

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+

+

1

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15th

Apply Defaults

7th

Meanwhile, on the electrical side it's quite common to assign a power net class filter to a rule. This allows you to ensure adequate space between objects on power nets and the rest of the board.



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